IN THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application.

1. (Previously Presented) A reconfigurable hardware apparatus to perform computational operations in one of a downsampling mode and a non-downsampling mode, comprising:

a plurality of adders, each of the plurality of adders including at least two inputs and one output;

a plurality of multipliers, each of the plurality of multipliers including at least two inputs and one output;

a switching fabric to switch between a downsampling mode of operation and a non-downsampling mode of operation, wherein the switching fabric is to provide for a configuration of the inputs and outputs of the adders with respect to the inputs and outputs of the multipliers; and,

a control logic block to control the switching fabric wherein in the non-downsampling mode, the switching fabric is to configure the multipliers and adders into a configuration that includes a plurality of MAAC kernels.

2. (Canceled)

3. (Previously Presented) The hardware apparatus according to claim 1, wherein in the downsampling mode, the switching apparatus is to configure the multipliers and adders into a configuration that includes the plurality of MAAC kernels and at least one AMAAC kernel.

4. (Previously Presented) The hardware apparatus according to claim 1 ~~2~~, wherein the MAAC kernel includes a multiplier block, an adder block and a register block, wherein an output of the multiplier block is coupled to an input of the adder block, an output of the adder block is coupled to an input of the register block and an output of the register block is coupled to a second input of the adder block and the adder block is to receive at its second input an additional addend.

5. (Previously Presented) The hardware apparatus according to claim 3, wherein the AMAAC kernel includes a multiplier block, a first adder block, a second adder block and a register block, wherein the first adder block is to receive two inputs (e(i) and a(i)) and an output of the first adder block is coupled to a first input of the multiplier block, the multiplier block is to receive a second input (b(i)) and an output of the multiplier block coupled to a first input of the second adder block, the second adder block is to receive a second input (c(i)) and an output of the second adder block is coupled to an input of the register block, an output of the register block coupled to a third input of the second adder block.

6. (Original) The hardware apparatus according to claim 1, wherein the computational operations include transformations.

7. (Original) The hardware apparatus according to claim 6, wherein the transformations include an inverse Discrete Cosine Transform (IDCT).

8. (Previously Presented) The hardware apparatus according to claim 7, wherein in the non-downsampling mode, an eight-point IDCT is to be computed utilizing the following expression:

$$\begin{bmatrix} x_0 \\ x_1 \\ x_2 \\ x_3 \end{bmatrix} = \frac{1}{2} A' \begin{bmatrix} y_0 \\ y_4 \\ y_2 \\ y_6 \end{bmatrix} + \frac{1}{2} B' \begin{bmatrix} y_1 \\ y_5 \\ y_3 \\ y_7 \end{bmatrix} \quad \begin{bmatrix} x_7 \\ x_6 \\ x_5 \\ x_4 \end{bmatrix} = \frac{1}{2} A' \begin{bmatrix} y_0 \\ y_4 \\ y_2 \\ y_6 \end{bmatrix} - \frac{1}{2} B' \begin{bmatrix} y_1 \\ y_5 \\ y_3 \\ y_7 \end{bmatrix}$$

where:

$$A' = \begin{bmatrix} 1 & 1 & c'(2) & c'(6) \\ 1 & -1 & c'(6) & -c'(2) \\ 1 & -1 & -c'(6) & c'(2) \\ 1 & 1 & -c'(2) & -c'(6) \end{bmatrix} \quad B = \begin{bmatrix} c'(1) & c'(5) & c'(3) & c'(7) \\ c'(3) & -c'(1) & -c'(7) & -c'(5) \\ c'(5) & c'(7) & -c'(1) & c'(3) \\ c'(7) & c'(3) & -c'(5) & -c'(1) \end{bmatrix}$$

9. (Previously Presented) The hardware apparatus according to claim 7, wherein in the downsampling mode, a 2:1 downsampling of an eight-point IDCT is to be computed utilizing the following expression:

$$\begin{bmatrix} x_0 \\ x_1 \\ x_2 \\ x_3 \end{bmatrix} = c(4) \begin{bmatrix} y_0 - y_7 + y_2 - y_5 + c'(2) * y_1 - c'(2) * y_6 + c'(6) * y_3 - c'6 * y_4 \\ y_0 - y_7 - y_2 + y_5 + c'(6) * y_1 - c'(6) * y_6 - c'(2) * y_3 + c'(2) * y_4 \\ y_0 - y_7 - y_2 + y_5 - c'(6) * y_1 + c'(6) * y_6 + c'(2) * y_3 - c'(2) * y_4 \\ y_0 - y_7 + y_2 - y_5 - c'(2) * y_1 + c'(2) * y_6 - c'(6) * y_3 + c'(6) * y_4 \end{bmatrix}.$$

10-18. (Canceled)

19. (Previously Presented) A method of performing computational operations, comprising:

providing a plurality of adders, each of the plurality of adders including at least two inputs and one output;

providing a plurality of multipliers, each of the plurality of multipliers including at least two inputs and one output;

controlling a switching fabric that provides for a configuration of the inputs and outputs of the adders with respect to the inputs and outputs of the multipliers so as to create a configuration that includes a plurality of MAAC kernals and switch between a downsampling mode of operation and a non-downsampling mode of operation.

20. (Previously Presented) The method of claim 19, wherein in said controlling operation, the switching fabric configures the multipliers and adders into a configuration that includes at least one AMAAC kernel.